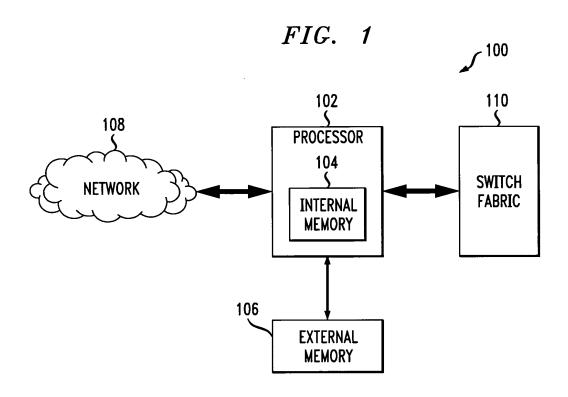
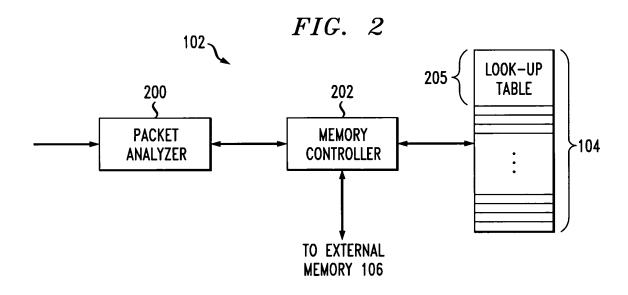
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Processor With Reduced Memory Requirements For High-Speed Routing And Switching Of Packets
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FIG. 3A

205	PORT 1	NUMBER OF BLOCKS
	PORT 2	NUMBER OF BLOCKS
	PORT 3	NUMBER OF BLOCKS
	PORT 4	NUMBER OF BLOCKS
	PORT 5	NUMBER OF BLOCKS
	PORT 6	NUMBER OF BLOCKS
		•
	PORT N	NUMBER OF BLOCKS
	L	_ <u></u>

FIG. 3B

05	PACKET FLOW 1	NUMBER OF BLOCKS
	PACKET FLOW 2	NUMBER OF BLOCKS
	PACKET FLOW 3	NUMBER OF BLOCKS
	PACKET FLOW 4	NUMBER OF BLOCKS
	PACKET FLOW 5	NUMBER OF BLOCKS
	PACKET FLOW 6	NUMBER OF BLOCKS
	•	•
		•
	PACKET FLOW N	NUMBER OF BLOCKS
•	<u> </u>	

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FIG. 4

